

## **DOPED ALUMINUM OXIDE DIELECTRICS**

### **RELATED APPLICATION**

**[0001]** This application is a continuation of U.S. Patent Application Serial No. 09/792,777 (allowed), filed February 23, 2001 and titled, "DOPED ALUMINUM OXIDE DIELECTRICS," which is commonly assigned and incorporated by reference in its entirety herein.

### **TECHNICAL FIELD OF THE INVENTION**

**[0002]** The present invention relates generally to dielectrics for integrated circuit devices, and in particular to the development of doped aluminum oxide dielectrics and devices containing such dielectrics.

### **BACKGROUND OF THE INVENTION**

**[0003]** To meet demands for faster processors and higher capacity memories, integrated circuit (IC) designers are focusing on decreasing the minimum feature size within integrated circuits. By minimizing the feature size within an integrated circuit, device density on an individual chip increases exponentially, as desired, enabling designers to meet the demands imposed on them. As modern silicon devices become smaller and the minimum feature size of CMOS (complementary metal oxide semiconductor) devices approaches and goes below the 0.1  $\mu\text{m}$  regime, very thin gate insulators of thickness less than 2 nm (20Å) will be required to keep the capacitance of the DRAM (dynamic random access memory) capacitor cell in the range of 30 fF. This capacitance value is generally required to provide immunity to radiation, soft errors and a nominal signal-to-noise ratio.

**[0004]** Silicon dioxide ( $\text{SiO}_2$ ), the most commonly used insulator, shows high leakage current density at thicknesses in the range of 20 nm due to band-to-band tunneling current or Fowler-Nordheim tunneling current. As a result, high-k dielectric films such as aluminum oxide ( $\text{Al}_2\text{O}_3$ ), tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) and titanium dioxide ( $\text{TiO}_2$ ) have received considerable interest as gate insulators to replace silicon dioxide.

**[0005]** While aluminum oxide has shown considerable promise, its porous nature leads to drawbacks. It has been noted that aluminum oxide porosity is generally the result of an acicular crystalline structure and that some pores may extend through the entire thickness of an aluminum oxide layer having a thickness on the order of 100 nm. Studies have also shown that exposure to humid atmospheres and even normal atmospheric conditions leads to a build-up of water in the pores of aluminum oxide films. This water build-up results in a loss of dielectric properties. In particular, water build-up can lead to a decrease in breakdown voltage of several orders of magnitude.

**[0006]** For the reasons stated above, and for other reasons stated below that will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternative aluminum oxide structures and methods of their production.

### **SUMMARY**

**[0007]** Aluminum oxide has shown considerable promise as a dielectric material for integrated circuit devices. However, its porous nature leads to drawbacks, in that the pores can adsorb water, thus resulting in a detrimental impact on the dielectric properties of the aluminum oxide material. The various embodiments of the invention involve a porous aluminum oxide layer having dopant material embedded in its pores and subsequently converted to a dielectric form. The doped aluminum oxide layer is formed sequentially to facilitate formation of a high-purity aluminum oxide layer and subsequently sealing its pores to impede water adsorption. Doped aluminum oxide layers of various embodiments are especially suited for use as gate dielectric layers, intergate dielectric layers and capacitor dielectric layers in various integrated circuit devices.

**[0008]** For one embodiment, the invention provides a doped aluminum oxide layer. The doped aluminum oxide layer includes an aluminum oxide layer having pores on a surface and a dopant material filling the pores. The dopant material is silicon, zirconium, hafnium or titanium and is applied to the aluminum oxide layer subsequent to a formation of the aluminum oxide layer.

**[0009]** For another embodiment, the invention provides a doped aluminum oxide layer. The doped aluminum oxide layer includes an aluminum oxide layer having pores on a surface and voids below the surface. The doped aluminum oxide layer further includes a dopant material of silicon, zirconium, hafnium or titanium. The pores contain at least a portion of the dopant material, and the voids are free of the dopant material.

**[0010]** For yet another embodiment, the invention provides a dielectric layer. The dielectric layer includes an aluminum oxide layer having pores on a surface and a second dielectric material embedded in the pores of the aluminum oxide layer. The second dielectric material is formed of a dopant material of silicon, zirconium, hafnium or titanium. The dopant material is embedded in the pores of the aluminum oxide layer and subsequently converted to its dielectric form.

**[0011]** For still another embodiment, the invention provides a dielectric layer. The dielectric layer includes an aluminum oxide layer having pores on a surface and voids below the surface. The dielectric layer further includes a second dielectric material. The second dielectric material is formed by depositing a dopant material in the pores and treating the dopant material to convert it to its dielectric form. The pores contain at least a portion of the second dielectric material, while the voids are free of the second dielectric material.

**[0012]** For one embodiment, the invention provides a method of forming a dielectric layer. The method includes forming a porous aluminum oxide layer on a substrate and forming a dopant layer on the porous aluminum oxide layer. The dopant layer contains a dopant material of silicon, zirconium, hafnium or titanium. The method further includes converting the dopant material to a dielectric form. For a further embodiment, excess dopant material is removed from the surface of the aluminum oxide layer prior to converting the dopant material to its dielectric form.

**[0013]** Further embodiments of the invention include apparatus and methods of varying scope.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0014]** Figures 1A-1C are cross-sectional views of a doped aluminum oxide layer taken during various processing stages in accordance with an embodiment of the invention.

**[0015]** Figure 1D is a cross-sectional view of one deposition system for use in forming the aluminum oxide layer of Figures 1A-1C.

**[0016]** Figure 2 is a cross-sectional view of a field-effect transistor in accordance with an embodiment of the invention.

**[0017]** Figure 3 is a cross-sectional view of a floating-gate field-effect transistor in accordance with an embodiment of the invention.

**[0018]** Figure 4 is a cross-sectional view of a portion of a DRAM memory array in accordance with an embodiment of the invention.

**[0019]** Figure 5 is a simplified block diagram of an integrated circuit memory device in accordance with an embodiment of the invention.

## **DETAILED DESCRIPTION**

**[0020]** In the following detailed description of the present embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that process, electrical or mechanical changes may be made without departing from the scope of the present invention. The terms wafer or substrate used in the following description include any base semiconductor structure. Examples include silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form

regions/junctions in the base semiconductor structure, and the terms wafer and substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

**[0021]** Figures 1A-1C depict fabrication of a doped aluminum oxide layer 108 as a portion of an integrated circuit device in accordance with one embodiment of the invention. Figures 1A-1C are cross-sectional views taken during various processing stages.

**[0022]** In Figure 1A an aluminum oxide layer 102 is formed on the substrate 100. The aluminum oxide layer 102 is porous, containing one or more pores 104 on the surface. Note that pores 104 may extend through the aluminum oxide layer 102 to the substrate 100 such as pore 104a. Voids 103 may be contained in the aluminum oxide layer 102. Voids 103 are spaces between grains or crystals of aluminum oxide that do not extend to the surface of the aluminum oxide layer 102.

**[0023]** The substrate 100 may be a monocrystalline silicon material. For example, the substrate 100 may be a wafer of monocrystalline silicon having a [100] orientation. The substrate 100 is generally a semiconductor material doped to a conductivity type, such as a p-type conductivity. As an example, the substrate 100 may be implanted with a p-type dopant, such as boron, followed by an anneal to produce a p-type substrate. As another example, the substrate 100 may have an n-type conductivity, such as a silicon substrate doped using an n-type dopant such as phosphorus or arsenic. Alternatively, the substrate 100 may be some other layer of an integrated circuit device. For example, the substrate 100 may be a floating gate layer of a floating-gate field-effect transistor. The substrate 100 may further include other semiconductor, conductor or insulator layers.

**[0024]** The aluminum oxide layer 102 is formed through physical vapor deposition (PVD) techniques to produce a high-purity film. The PVD techniques preferably are evaporation techniques using a high-purity aluminum or alumina source, such as zone-refined aluminum or sapphire crystals. Such sources are significantly more pure than traditional powder targets commonly used in PVD sputtering techniques. For one embodiment, the aluminum or alumina source has a purity in excess of 99.99%. For a

further embodiment, the aluminum or alumina source has a purity of approximately 99.9999%. Evaporation PVD techniques are well understood in the art. Examples include thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition. For aluminum sources, formation of an aluminum oxide layer 102 would require reactive evaporation of the aluminum source in an oxygen-containing atmosphere, a technique well known in the art.

[0025] The level of porosity of the aluminum oxide layer 102 may be expressed as packing density. Packing density,  $p$ , is a measure of the extent individual grains or crystals of aluminum oxide occupy the gross volume of the aluminum oxide layer 102 relative to voids or pores. Packing density has been defined in literature by the relation:

$$p = \sigma / (\rho_{sc}h)$$

where:  $\sigma$  is the surface density of the layer;

$\rho_{sc}$  is the volume density of the skeleton of the film; and

$h$  is the geometric height of the film

As a first approximation,  $\rho_{sc}$  can be equated to the density of sapphire, or 3.99 g/cm<sup>3</sup>.

[0026] Wide ranges of packing density are readily producible in aluminum oxide films as has been reported in the literature. *See, e.g.,* Brik, E.B., "Effect of Substrate Temperature on Density of Aluminum Oxide Films," Opt. Mekh. Promst. 57 (1), pp. 50-52 (January 1990) (reporting packing density values ranging from 0.66 to 0.95). Vacuum-deposited aluminum oxide films on cold substrates are generally amorphous while an acicular crystalline structure appears at higher substrate temperatures. *Id.*

[0027] The degree of packing density can be easily controlled through the use of ion bombardment or plasma activation during deposition. As demonstrated in one study, packing density of electron-beam evaporated aluminum oxide films can be controlled through oxygen ion bombardment during deposition. In this study, the index of refraction, and therefore the film density, first rose and then decreased with increasing ion current density for substrate temperatures between 70°C and 250°C. *See, Franzen, W., et al., "Study of Oxygen-Ion-Beam-Assisted Evaporated Aluminum Oxide Films," Mat. Res.*

Soc. Symp. Proc., Vol. 29, pp. 825-30 (1993). Similarly, the addition of plasma activation during film deposition has been shown to produce a glassy fracture and denser microstructure than film deposition without plasma activation. *See*, Zywitzki, O., et al., "Effect of Plasma Activation on the Phase Transformations of Aluminum Oxide," Surface and Coatings Tech. 76-77, pp. 745-762 (1995).

[0028] The aluminum oxide layer 102 is a porous layer having a packing density of less than 1. For one embodiment, the aluminum oxide layer 102 has a packing density of between approximately 0.65 and 0.999. For a further embodiment, the aluminum oxide layer 102 has a packing density of between approximately 0.85 and 0.999.

[0029] The aluminum oxide layer 102 is doped, subsequent to deposition or formation, to improve the dielectric properties of the resultant film. In Figure 1B, a dopant layer 106 is formed on the aluminum oxide layer 102. The dopant layer 106 contains a dopant material. For one embodiment, the dopant layer 106 contains silicon (Si). For additional embodiments, the dopant layer 106 may contain zirconium (Zr), titanium (Ti) or hafnium (Hf). The dopant layer 106 fills pores 104 of the aluminum oxide layer 102 and covers the surface of the aluminum oxide layer 102.

[0030] The dopant layer 106 may be formed by PVD or chemical vapor deposition (CVD) techniques as a blanket deposition. As one example, a silicon-containing dopant layer 106 may be formed by CVD using silane ( $\text{SiH}_4$ ) or other suitable silicon precursor. For one embodiment, a dilute silane feed, e.g., 2% silane in nitrogen ( $\text{N}_2$ ), is pulsed into a reaction chamber for deposition of the dopant layer 106 on the aluminum oxide layer 102. The dopant layer 106 is deposited to a thickness less than or equal to an average diameter of the pores 104 using a substrate temperature of approximately 300°C to 350°C. This process is similar to the passivation of a copper substrate by silicide formation as provided in Hymes, S., et al., "Passivation of Copper by Silicide Formation in Dilute Silane," Mat. Res. Soc. Conf. Proc., ULSI-VII, pp. 425-31 (1992). For a further embodiment, the dopant layer 106 is deposited to a thickness of less than approximately 5 nm.

[0031] In Figure 1C, excess dopant material is optionally removed from the surface of the aluminum oxide layer 102. This leaves islands 107 of dopant material, i.e., that

material filling the pores 104, embedded in the surface of the aluminum oxide layer 102. For one embodiment, removal of excess dopant involves exposing the surface of the dopant layer 106 to a mild ion beam, such as a beam of argon (Ar) ions. Removal of excess dopant material can eliminate the series capacitance effects of two adjacent dielectric layers.

**[0032]** For one embodiment, the aluminum oxide layer 106 has a packing density such that the dopant material embedded in the surface of the aluminum oxide layer 102, e.g., the islands 107 of dopant material, constitutes approximately 0.1% to 30% by weight of the doped aluminum oxide layer 108. For a further embodiment, the aluminum oxide layer 106 has a packing density such that the dopant material embedded in the surface of the aluminum oxide layer 102 constitutes approximately 0.1% to 10% by weight of the doped aluminum oxide layer 108.

**[0033]** Whether or not the excess dopant material is removed, the dopant material is subsequently treated to homogenize the doped aluminum oxide layer 108. Such treatment of the dopant material can include oxidation or nitridation to convert the dopant material to its oxide or nitride form appropriate to impart dielectric properties to the dopant material.

**[0034]** For one embodiment, the dopant material is oxidized by rapid thermal annealing in an oxidizing atmosphere, such as an oxygen-containing atmosphere. The oxygen-containing atmosphere should preferably contain sufficient oxygen to oxidize all of the dopant material. For example, for a dopant layer 106 containing silicon, the oxygen-containing atmosphere should contain sufficient oxygen to convert all of the silicon, i.e., the dopant layer 106 or the islands 107 of dopant material, to silicon dioxide. For other embodiments, the treated dopant material includes zirconium dioxide (ZrO<sub>2</sub>), hafnium dioxide (HfO<sub>2</sub>) or titanium dioxide (TiO<sub>2</sub>), formed by oxidation of zirconium, hafnium or titanium dopant materials, respectively.

**[0035]** For another embodiment, the dopant material is nitrided by rapid thermal nitridation in a nitrogen-containing atmosphere. The nitrogen-containing atmosphere should preferably contain sufficient nitrogen to nitride all of the dopant material. For example, for a dopant layer 106 containing silicon, the nitrogen-containing atmosphere



should contain sufficient nitrogen to convert all of the silicon, i.e., the dopant layer 106 or the islands 107 of dopant material, to silicon nitride ( $\text{Si}_3\text{N}_4$ ).

[0036] Figure 1D is a cross-sectional view of one deposition system 112 for use in forming an aluminum oxide layer 102 as described above. The deposition system 112 includes a chamber 114 for containing the substrate 100 under vacuum. A crucible 118 holds an aluminum or alumina source 122. The source 122 is heated, e.g., by resistive heating or electron-beam bombardment, to produce vaporized species 124 for deposition on a surface of the substrate 100. If the vaporized species 124 are aluminum atoms, they may be reacted with an oxygen-containing atmosphere within the chamber 114 to produce aluminum oxide.

[0037] An ion gun 126 may be included in the deposition system 112 to provide ion beams 132 impinging on the surface of the substrate 100. The ion beams 132 generally impinge on the surface of substrate 100 at some angle, e.g., approximately  $20^\circ$ . A gas inlet 128 provides an ion source for the ion gun 126, e.g., oxygen or argon to produce oxygen ions and argon ions, respectively. For plasma activation of the vaporized species 124, a plasma 134 is formed between the crucible 118 and the substrate 100.

[0038] The doped aluminum oxide layer 108 may be used as a dielectric layer in a variety of integrated circuit devices subsequent to converting the dopant material to its dielectric form. Example uses include gate dielectric layers for field-effect transistors, intergate dielectric layers for floating-gate transistors and capacitor dielectric layers. The doped aluminum oxide layer 108 differs from layers of aluminum oxide that are doped during deposition in that the dopant material is not dispersed throughout the layer. The evaporation PVD techniques facilitate use of high-purity sources. The evaporation PVD techniques further facilitate control over the degree of porosity, and thus the dopant level, of the resultant layer.

[0039] Figure 2 is a cross-sectional view of a field-effect transistor having a gate stack 245 overlying a substrate 200, a first source/drain region 235 in the substrate 200 adjacent a first sidewall of the gate stack 245, and a second source/drain region 240 in the substrate 200 adjacent a second sidewall of the gate stack 245. The gate stack 245 includes a gate

dielectric layer 205. The gate dielectric layer 205 contains a doped aluminum oxide layer in accordance with an embodiment of the invention. Gate stack 245 further includes a conductor, often containing a conductively-doped polysilicon layer 210 overlying the gate dielectric layer 205, a metal layer 220, and a conductive barrier layer 215 interposed between the polysilicon layer 210 and the metal layer 220. Insulative cap layer 225 and sidewall spacers 230 insulate and protect the gate stack 245 from other adjacent layers. The field-effect transistor of Figure 2 may be an access transistor of a DRAM memory cell, having the first source/drain region 235 coupled to a bit line and the second source/drain region 240 coupled to a cell capacitor.

**[0040]** Figure 3 is a cross-sectional view of a floating-gate field effect transistor, or simply a floating-gate transistor, having a gate stack 345 overlying a substrate 300, a first source/drain region 335 in the substrate 300 adjacent a first sidewall of the gate stack 345, and a second source/drain region 340 in the substrate 300 adjacent a second sidewall of the gate stack 345. The gate stack 345 includes a gate dielectric layer 305. For one embodiment, the gate dielectric layer 305 contains a doped aluminum oxide layer in accordance with an embodiment of the invention. Gate stack 345 further includes a floating-gate layer 311, a control-gate layer 321 and an intergate dielectric layer 317 interposed between the floating-gate layer 311 and the control-gate layer 321. For one embodiment, the intergate dielectric layer 317 contains a doped aluminum oxide layer in accordance with an embodiment of the invention.

**[0041]** Insulative cap layer 325 and sidewall spacers 330 insulate and protect the gate stack 345 from other adjacent layers. The floating-gate transistor of Figure 3 may be a flash memory cell, having the first source/drain region 335 coupled to a bit line of a flash memory array and having at least the control-gate layer 321 coupled to a word line of the flash memory array. The second source/drain region 340 is generally commonly coupled among all memory cells of the flash memory array or a portion of the flash memory array.

**[0042]** Figure 4 is a cross-sectional view of a portion of a DRAM memory array. The memory array includes word lines 445a as access transistors overlying the substrate 400. Word lines 445b are formed overlying isolation regions 495 and are coupled to access

transistors for memory cells outside the plane of the drawing. Each memory cell of the DRAM memory array includes an access transistor and a cell capacitor.

[0043] Each word line 445a has a first source/drain region 435 coupled to a bit line 485 through a bit-line contact 490. Each word line 445a further has a second source/drain region 440 coupled to a first plate 455 of a cell capacitor, such as through a conductive plug 450. The cell capacitor has a second plate 470 and a cell dielectric layer 465 interposed between the first plate 455 and the second plate 470. The second plate 470, or cell plate, is generally shared among all memory cells of the memory array or a portion of the memory array. Insulating layer 480 provides structural support to the cell capacitors as well as electrical isolation of adjacent conductive layers.

[0044] For one embodiment, the cell dielectric layer 465 contains a doped aluminum oxide layer in accordance with an embodiment of the invention. For another embodiment, the word lines 445a contain a doped aluminum oxide gate dielectric layer in accordance with an embodiment of the invention.

[0045] Figure 5 is a simplified block diagram of an integrated circuit memory device 500 in accordance with an embodiment of the invention. The memory device 500 may include a DRAM device or a flash memory device. The memory device 500 includes an array of memory cells 502, an address decoder 504, row access circuitry 506, column access circuitry 508, control circuitry 510, and Input/Output (I/O) circuitry 512. For a DRAM memory device, the memory array 502 contains memory cells having an access transistor coupled between a bit line and a capacitor. For a flash memory device, the memory array 502 contains flash memory cells having a floating-gate transistor coupled to a bit line.

[0046] The memory device 500 can be coupled to a processor 514 or other memory controller for accessing the memory array 502. The memory device 500 coupled to a processor 514 forms part of an electronic system. Some examples of electronic systems include personal computers, peripheral devices, wireless devices, digital cameras, personal digital assistants (PDAs) and audio recorders.

**[0047]** The memory device 500 receives control signals across control lines 516 from the processor 514 to control access to the memory array 502. Access to the memory array 502 is directed to one or more target memory cells in response to address signals received across address lines 518. Once accessed in response to the control signals and the address signals, data is written to or read from the memory cells across DQ lines 520.

**[0048]** The memory cells of the memory array 502 are generally arranged in rows and columns with a memory cell located at each intersection of a bit line and a word line. Those memory cells coupled to a single word line are generally referred to as a row of memory cells while those memory cells coupled to a single bit line are generally referred to as a column of memory cells. The array of memory cells 502 includes at least one memory cell having a gate dielectric layer, an intergate dielectric layer or a capacitor dielectric layer in accordance with the invention.

**[0049]** It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of Figure 5 has been simplified to help focus on the invention. It will be understood that the above description of a memory device is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a typical memory device.

**[0050]** As recognized by those skilled in the art, memory devices of the type described herein are generally fabricated as an integrated circuit containing a variety of semiconductor devices. The integrated circuit is supported by a substrate. Integrated circuits are typically repeated multiple times on each substrate. The substrate is further processed to separate the integrated circuits into dies as is well known in the art.

**[0051]** The foregoing figures were used to aid the understanding of the accompanying text. However, the figures are not drawn to scale and relative sizing of individual features and layers are not necessarily indicative of the relative dimensions of such individual features or layers in application. Accordingly, the drawings are not to be used for dimensional characterization.

## **CONCLUSION**

**[0052]** Aluminum oxide has shown considerable promise as a dielectric material for integrated circuit devices. However, its porous nature leads to drawbacks in that the pores can adsorb water, thus resulting in a detrimental impact on the dielectric properties of the aluminum oxide material. The various embodiments of the invention involve a porous aluminum oxide layer having dopant material embedded in its pores and subsequently converted to a dielectric form. The doped aluminum oxide layer is formed sequentially to facilitate formation of a high-purity aluminum oxide layer and subsequently sealing its pores to impede water adsorption. Doped aluminum oxide layers of various embodiments are especially suited for use as gate dielectric layers, intergate dielectric layers and capacitor dielectric layers in various integrated circuit devices.

**[0053]** Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. For example, other materials, shapes, deposition techniques and removal techniques may be utilized with the invention. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.